



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/585,643

07/07/2006

Takanori Okada

056937-0295

5463

53080 7590 03/09/2011  
MCDERMOTT WILL & EMERY LLP  
600 13TH STREET, NW  
WASHINGTON, DC 20005-3096

EXAMINER

GIARDINO JR, MARK A

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

03/09/2011

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/585,643

Applicant(s)

OKADA ET AL.

Examiner

MARK A. GIARDINO JR

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 February 2010.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2,4,8,10,14 and 16 is/are allowed.
- 6) ☐ Claim(s) 1, 3, 5-7, 9, 11-13, 15, 17, and 18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/9/2010 has been entered.

The instant application having Application No. 10/585,643 has a total of 18 claims pending in the application, there are 18 independent claims, all of which are ready for examination by the examiner.

**REJECTIONS BASED ON PRIOR ART**

**Claim Rejections - 35 USC ' 102**

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6, 12, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba (US 6,401,166).

**Regarding Claim 6**, Chiba teaches a non-volatile semiconductor recording medium (**memory card 40 of Figure 3**) in which information is recorded according to a

Art Unit: 2185

recording format of FAT file system (**Chiba uses the FAT file system, which uses “a table indicating an allocation of the file”, Column 8 Lines 64-67),**

wherein a user data region comprising a plurality of clusters (**data regions of Figure 4, which also shows a plurality of clusters among the data regions**) and a file allocation table region (**FAT region of Figure 4**) are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region (**since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT inherently records information on the state of the clusters, Column 14 Lines 3-11**);

the file allocation table region indicates that a continuous series of at least two hundred clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster (**The FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-11, also see step S504 of Figure 11, and Chiba states that a cluster is the “minimum unit of a file”, Column 8 Lines 50-54, therefore the FAT file system inherently teaches storing files of any particular size, encompassing a size of 200 clusters**),

and a region of the user data region corresponding to the continuous series of at least 200 clusters is physically erased (**see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”, and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased,**

**see Format processing information on Column 12 Line 52 to Column 13 Line 25).**

**Claim 12** is the method equivalent of claim 6, and is rejected under similar rationale.

**Claim 18** is the information recording format equivalent of claim 6, and is rejected under similar rationale.

**Claim Rejections - 35 USC ' 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1, 3, 7, 9, 13, and 15 are rejected** under 35 U.S.C. 103(a) as being unpatentable over **Chiba (US 6,401,166) in view of Kozaki et al (US 6,788,575).**

**Regarding Claim 1**, Chiba teaches a recording medium of non-volatile semiconductor **(memory card 40 of Figure 3)** comprising:

a plurality of blocks, each block being a first size and physically erasable as a single unit **(Chiba teaches the flash is erasable by blocks, where each block is erasable as a single unit, Column 1 Line 17-24);**

a partition management information region **(master boot memory region of**

**Figure 4 in Chiba)** and

a partition region **(starting with partition boot memory region of Figure 4)**,  
wherein

an information on a start position of the partition region is recorded in the partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**,

the start position information includes a value at which a predetermined region **(the predetermined region being the "empty region" of Figure 4)** is secured between a terminal end of the partition management information region and a starting end of the partition region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] is secured, Column 8 Lines 27-32, where "secured" is given the meaning of "established for a particular purpose" as it is used in the specification).**

However, Chiba does not explicitly teach the region secured between the terminal end of the partition management information region is larger than 200 times the first size and the starting end of the partition region is in a state where data is physically erased. Kozaki teaches an alternative area **(shown in Figure 2)** between a management table and a regular data area which is larger than 200 times the erasable unit size **(the maximum number of alternative sectors is variable, Column 6 Line**

Art Unit: 2185

**64 to Column 7 Line 18, and sectors are the unit of erasing, Column 17 Lines 20-25, and there are at least 200 sectors since a “segment” consists of 128 sectors in the embodiment described, Column 4 Line 61 to Column 5 Line 8) in a state where data is physically erased (since the alternative segments map only defective sectors, Column 6 Lines 18-34, data is physically erased until one of the sectors in the alternative segment is used for data storage).**

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have secured (where “secured” is given the meaning of “established for a particular purpose” as it is used in the specification) the alternative region between the terminal end of the partition management information region and a starting end of the partition region (as in Kozaki) in the device of Chiba, in order to replace defective memory blocks while keeping the memory system operable (Column 1 Lines 49-67 in Kozakai).

**Claim 7** is the method equivalent of claim 1, and is rejected under similar rationale.

**Claim 13** is the information recording format equivalent of claim 1, and is rejected under similar rationale.

**Regarding Claim 3**, Chiba teaches a non-volatile semiconductor recording medium (**flash memory 1 of Figure 1**) comprising:

a plurality of erasing blocks, each erasing block being of a first size and physically erasable as a single unit (**Chiba teaches the flash is erasable by blocks,**

Art Unit: 2185

**where each block is erasable as a single unit, Column 1 Line 17-24); wherein**

information is recorded according to a recording format of a predetermined file system **(FAT file system format, which uses “a table indicating an allocation of the file”, Column 8 Lines 64-67),**

However, Chiba does not explicitly teach a region which is not used for the recording is larger than 200 times the first size and is included in the recording format of the file system, and the region which is not used for the recording is in a state where data is physically erased. Kozaki teaches an alternative area **(shown in Figure 2)** between a management table and a regular data area which is larger than 200 times the erasable unit size **(the maximum number of alternative sectors is variable, Column 6 Line 64 to Column 7 Line 18, and sectors are the unit of erasing, Column 17 Lines 20-25, and there are at least 200 sectors since a “segment” consists of 128 sectors in the embodiment described, Column 4 Line 61 to Column 5 Line 8)** in a state where data is physically erased **(since the alternative segments map only defective sectors, Column 6 Lines 18-34, data is physically erased until one of the sectors in the alternative segment is used for data storage).**

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the alternative region (as in Kozaki) in the device of Chiba, in order to replace defective memory blocks while keeping the memory system operable (Column 1 Lines 49-67 in Kozakai).



**Claim 9** is the method equivalent of claim 3, and is rejected under similar rationale.

**Claim 15** is the information recording format equivalent of claim 3, and is rejected under similar rationale.

Claims 5, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba and Kozaki in further view of Nakamura et al (US 6,873,789).

**Regarding Claim 5**, Chiba teaches a non-volatile semiconductor recording medium of non-volatile semiconductor (**flash memory 1 of Figure 1**) comprising:

a plurality of blocks, each block being a first size and physically erasable as a single unit (**Chiba teaches the flash is erasable by blocks, where each block is erasable as a single unit, Column 1 Line 17-24**);

A partition management information region (**master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26**);

and a partition containing a file system specific region (**Chiba uses the FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Lines 64-67**),

an information on a start position of the space bit map region is recorded in the partition descriptor information region (**the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32**),

the partition comprises a partition descriptor information region (**partition boot memory region of Figure 4**);

an information on a start position of the space bit map region is recorded in the partition descriptor information region (**master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26**);

However, Chiba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system (**Column 6 Lines 22-25**) with a space bit map in memory (**Column 12 Lines 52-53**). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chiba and to use a UDF file system in place of the FAT file system, so that the memory device of Chiba can be compatible with operating systems that use the UDF file system.

Also, neither Chiba nor Nakamura explicitly teach the start position information includes a value at which a predetermined region larger than 200 times the first size included in the partition is secured prior to a starting end of the space bit map region, and the region secured prior to the starting end of the space bit map region is in a state where data is physically erased. Kozaki teaches an alternative area (**shown in Figure 2**) between a management table and a regular data area which is larger than 200 times the erasable unit size (**the maximum number of alternative sectors is variable, Column 6 Line 64 to Column 7 Line 18, and sectors are the unit of erasing, Column 17 Lines 20-25, and there are at least 200 sectors since a "segment"**

Art Unit: 2185

**consists of 128 sectors in the embodiment described, Column 4 Line 61 to Column 5 Line 8) in a state where data is physically erased (since the alternative segments map only defective sectors, Column 6 Lines 18-34, data is physically erased until one of the sectors in the alternative segment is used for data storage).**

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have secured (where “secured” is given the meaning of “established for a particular purpose” as it is used in the specification) the alternative region (as in Kozaki) in the device of Chiba and Nakamura, in order to replace defective memory blocks while keeping the memory system operable (Column 1 Lines 49-67 in Kozakai).

**Claim 11** is the method equivalent of claim 5, and is rejected under similar rationale.

**Claim 17** is the information recording format equivalent of claim 5, and is rejected under similar rationale.

## **ARGUMENTS CONCERNING PRIOR ART REJECTIONS**

### **Rejections - USC 102/103**

Applicant’s arguments regarding Claims 1, 3, 7, 9, 13, and 15 have been considered but are moot in view of the new grounds of rejection.

Applicant’s argument regarding Claims 6, 12, and 18 that Chiba does not teach

Art Unit: 2185

“a continuous series of at least 200 clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster, or an already-used cluster; and a region of the user data region corresponding to the continuous series of at least 200 clusters is physically erased” has been considered but is not persuasive. Chiba teaches erasing the user data region (see step s401 in Figure 10, where there is a command to “erase each block and then erase the storage content of each block”) thus including a region of the user data region corresponding to the continuous series of at least two hundred clusters.

During use, the clusters are used for file storage and the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if two hundred continuous clusters are used (which is inherently taught by the FAT file system, which can incorporate files of any number of clusters) the file allocation table region would indicate that a continuous series of at least two hundred clusters are used. This satisfies the limitations of claims 6, 12, and 18. Chiba teaches the limitations of Claims 6, 12, and 18 to the extent that they are claimed.

## **CLOSING COMMENTS**

### **Conclusion**

## **STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

**SUBJECT MATTER CONSIDERED ALLOWABLE**

Claims 2, 8, 14, 4, 10, and 16 have been considered allowable subject matter.

**CLAIMS REJECTED IN THE APPLICATION**

Per the instant office action, claims 1, 3, 5, 6, 7, 9, 11, 12, 13, 15, 17, and 18 have received a first action on the merits and are subject of a first action non-final.

**DIRECTION OF FUTURE CORRESPONDENCES**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571) 270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/Stephen Elmore/  
Primary Examiner, Art Unit 2185

/M.G./

Patent Examiner  
Art Unit 2185

March 8, 2011